High-Performance Bottom-Contact Organic Thin-Film Transistors with Controlled Molecule-Crystal/Electrode Interface**

By Mingsheng Xu,* Masakazu Nakamura,* Masatoshi Sakai, and Kazuhiro Kudo

Organic thin-film transistors (OTFTs) are emerging as an inexpensive alternative to amorphous silicon devices because of their many attractive features, such as a simple fabrication process, low cost, and mechanical flexibility. Recently, the performance of OTFTs has been significantly improved by modifying the dielectric surface and/or source and drain (S/D) electrodes,[1] or by using novel dielectric materials.[2–5] However, high-performance OTFTs were mostly achieved in top-contact (TC) configurations[6] and not in bottom-contact (BC) configurations. As organic active materials are sensitive to chemical wet and ion-beam processes, shadow-mask evaporation is usually used to form S/D electrodes in TC configurations. Such a process, however, is incompatible with large-scale integration and does not allow one to produce a channel length shorter than a few tens of micrometers. It is therefore desirable to use a BC configuration, which is compatible with fine lithography processing, for promising applications such as high-resolution flexible displays.

The performance of OTFTs is mainly dependent on i) molecular ordering in the organic active layer, ii) charge-injection ability of the source electrode, and iii) charge transport at the interface between the organic active layer and the dielectric layer; the inferior performance of BC-OTFTs compared with TC counterparts is believed to mostly derive from factors (i) and (ii). The step formed by S/D electrodes, in particular thick S/D electrodes on a dielectric layer, disturbs the continuous growth of a single-phase domain in the organic active layer.[7] Additionally, electrode edges with a relatively irregular shape may cause disordered growth of organic crystals adjacent to the electrodes. Despite this, not much effort is required to overcome the inherent drawbacks. A simple approach to completely eliminate the electrode-induced effects in BC-OTFTs is to embed the S/D electrodes in the dielectric layer and planarize the S/D electrodes, making the S/D electrodes and dielectric layer coplanar.

In this Communication, we report, for the first time, planarized BC-OTFTs (pBC-OTFTs) with S/D electrodes embedded in the dielectric layer (Fig. 1a); this led to a preferential orientation of organic crystals adjacent to the S/D electrodes and a continuous growth of organic crystals across the S/D edges. Our pentacene pBC transistors on SiO2/Si showed a superior performance in controlling conventional BC-OTFTs (cBC-OTFTs) (Fig. 1d) and TC-OTFTs, and the mobility was comparable with the best value ever reported for TC-OTFTs made with similar materials.

We investigated bottom-gate pBC-OTFTs and cBC-OTFTs built on a SiO2/Si platform. In the present study, Pt (ca. 31 nm)/Cr (ca. 2 nm) were used as the S/D electrodes, and pentacene thin films, fabricated by using the molecular-beam-deposition technique,[8,9] were used as the active organic semiconductor. The width and length of our transistors was 5000 and 22.9 μm, respectively. We tested eight devices for each type of transistor and show the properties of the device with the best mobility obtained. As shown in Figure 1b, the current–voltage characteristics of a representative pentacene pBC transistor showed a strong field-effect modulation of the channel conductance. By fitting the data to the linear-saturation-regime standard field-effect transistor equations,[7] the linear and saturation mobilities were estimated to be 0.36 cm2 V–1 s–1 (the bias applied between the drain and the source electrodes Vds = –20 V) and 0.48 cm2 V–1 s–1 (Vds = –80 V), respectively. In contrast, the linear and saturation mobilities of the control cBC transistor (Fig. 1e) are 0.17 cm2 V–1 s–1 (Vds = –20 V) and 0.30 cm2 V–1 s–1 (Vds = –80 V), respectively. Thus, the linear mobility of the pBC-OTFT is more than twice that of the cBC-OTFT. Furthermore, the mobility of our pentacene pBC-OTFT is higher than that of our TC counterpart with Au as the S/D electrodes (see Table 1) and comparable with the best values for that of TC-OTFTs fabricated with similar materials, reported to date (which is typically around 0.5 cm2 V–1 s–1).[5,10] All our transistors showed a gate leakage current less than a nanoampere. In addition, the magnitude of the on-state drain current of the pBC-OTFT was about twice that of the control transistors (see Table 1). This sort of high-saturation mobility and large current is necessary to drive organic light-emitting diodes. The device with planar S/D electrodes had high mobility, improving the state of the art, at least for BC-OTFTs on SiO2/Si without surface modification. By modifying the dielectric surface using a self-assembled monolayer, treating the
Figure 1. a) A schematic illustration of a pBC-OTFT configuration. b) Output characteristics of the pentacene (ca. 66 nm) pBC-OTFT; the corresponding atomic force microscopy (AFM) topographic image is shown in Figure 2c. c) The output characteristics in the small bias range of (b). d) A schematic illustration of a cBC-OTFT configuration. e) Output characteristics of the pentacene (ca. 99 nm) cBC-OTFT; the corresponding AFM topographic image is shown in Figure 2f. f) The output characteristics in the small bias range of (e).

Table 1. A summary of the main parameters of the pentacene planarized (p) and conventional (c) BC-OTFTs, as well as the TC-OTFT. \( \mu \) is the mobility and \( V_T \) is the threshold voltage. The gate leakage current of all the transistors was less than 1 nA.

<table>
<thead>
<tr>
<th>OTFT</th>
<th>( \mu ) [( \text{cm}^2\text{V}^{-1}\text{s}^{-1} )] @ –20 V</th>
<th>( \mu ) [( \text{cm}^2\text{V}^{-1}\text{s}^{-1} )] @ –80 V</th>
<th>( V_T ) [V]</th>
<th>On-state current [( \mu A )][[d]]</th>
</tr>
</thead>
<tbody>
<tr>
<td>pBC</td>
<td>0.36</td>
<td>0.48</td>
<td>–3.5</td>
<td>–2.86</td>
</tr>
<tr>
<td>cBC</td>
<td>0.17</td>
<td>0.30</td>
<td>–5.2</td>
<td>–1.61</td>
</tr>
<tr>
<td>TC</td>
<td>0.25</td>
<td>0.35</td>
<td>–12</td>
<td>–1.27</td>
</tr>
</tbody>
</table>

[a] Pt/Cr as the S/D electrodes; the thickness of the pentacene was ca. 66 nm. [b] Pt/Cr as the S/D electrodes; the thickness of the pentacene was ca. 99 nm. [c] Au as the S/D electrodes; the thickness of the pentacene was ca. 99 nm. [d] @ \( V_{ds} = –100 \) V and \( V_g \) (the bias applied to gate electrode) = –60 V.

...surface with \( \text{O}_2 \) plasma or \( \text{UV/O}_3 \), and/or optimizing the device fabrication procedure, we believe that the performance of pBC-OTFTs could be further improved. We recognize that the high performance of our BC transistors (both pBC and cBC without surface modification, Fig. 2c and f) was mainly because the spikes at the edges of the S/D electrodes next to the high-quality pentacene grains were removed. A spike is commonly observed at the edges of S/D electrodes (see Fig. 2b and e) formed by using conventional photolithography and lift-off processes. We found that spikes seriously affected the growth of the organic active film and in turn device performance (not shown here).

Compared with cBC-OTFTs, the improvement of the field-effect properties of pBC-OTFTs is primarily attributed to the preferential orientation of the pentacene grains near the edges of the S/D electrodes, which improves electric-contact ability at the interface between the S/D electrodes and the channel. To illustrate this point, we statistically analyzed the orientation distribution of the long-axis of 111 pentacene grains adjacent to the S/D electrodes (Fig. 3) and probed the pentacene molecular packing in the grains (Fig. 4). Figure 3a suggests that the long axis of the pentacene grains in the pBC configuration (a Gaussian fit gives a peak at 89.6° and a full width at half maximum of 4.2°) was mostly normal to the edge of the S/D electrodes (e.g., see Fig. 2b), with approximately 55 % of the grains aligned within a 80–100° range, in strong contrast to the nearly random distribution of the pentacene grains (e.g., see Fig. 2e) in the cBC configuration, as shown in Figure 3b (a Gaussian fit gave a peak at 88.6° and a full width at half maximum of 59.5°). Furthermore, we obtained, for the first time, molecule-resolution images from isolated grains in the real device (Fig. 4), which helped to determine the molecular-packing structure in the diamond-shaped grain on SiO2. The contact-mode atomic force microscopy (AFM) topographic image in Figure 4a shows the grains near the S/D electrode (top part of the image). The friction-force images (Fig. 4b–d), obtained from the locations 1–3 marked in Figure 4a, show the corresponding molecular-packing structures in the grains. Based on the images, we determined the pentacene unit cells as seen in Figure 4e–g. These results are consistent with a molecular-packing motif resembling the \( ab \)-plane of the bulk form, although the characteristic unit-cell dimensions (see the caption of Fig. 4; the error might be up to 10% because of sample drift and scanner calibration) show little difference from the corresponding lattice parameters reported for both the bulk form and various thin-film phases. Our results indicated that the long axis of the diamond-shaped pentacene grain was along the \( b \)-vector, and that the growth front of the grain (which is the same as the sides of the diamond shape) became \{1110\} molecular steps (Fig. 5).

As the electrode edges in both pBC and cBC configurations themselves did not exhibit an apparent difference in shape, the driving force of the preferential orientation of the pentacene grains in the pBC configuration was considered to origi-
nate from the ‘folding line’ of the SiO₂ surface formed from the isotropic etching, as seen in Figure 2a. This straight folding line restricted the in-plane orientation of the pentacene nuclei by causing the [100] direction, where molecules were aligned with the same inclination direction and with high density, to be parallel to the folding line (and the edge of electrode) in the initial stages of the film growth (see Fig. 5). This could be regarded as a kind of grapho-epitaxy. A similar concept of orientation control has been reported when using a regularly stepped surface. Also, the folding angle is small enough (ca. 6°) not to interrupt the continuity of the crystals across the line. Based on the above analyses, the preferential orientation of elongated grains adjacent to the S/D edges could form a perfect contact at the electrode/channel interface through effective π-orbital overlapping between the S/D electrodes and the ac-plane of the pentacene grains (where the plane is topologically flat and has a high molecule density), and thus reduce the contact resistance and interfacial trap density.

Another reason why there was an improvement was the existence of grains overlapping at the S/D edges (see inset in Fig. 2b and the marked grains in Fig. 2c). The overlap improved the continuity of the pentacene grains across the edges of the S/D electrodes, enhancing charge injection and transport abilities at the electrode/channel interface. In the case of the cBC configuration (Fig. 2d–f and the topographic profiles in Fig. 2g–i), we can see that the pentacene grains at the interface between the S/D electrode and the dielectric layer

**Figure 2.** Tapping-mode AFM topographic images. The image size in (a) and (d) is 5 μm × 5 μm, and it is 10 μm × 10 μm in the other panels. a) The embedded S/D electrode in the pBC configuration. b) Ca. 4 nm pentacene in the pBC configuration with an inset (ca. 3 nm pentacene, 2.7 μm × 2.7 μm) showing molecules across the S/D edge and folding line (high-pass filtered). c) Ca. 66 nm pentacene in the pBC configuration. d) The S/D electrode in a cBC configuration. e) Ca. 4 nm pentacene in the cBC configuration with an inset (ca. 3 nm pentacene, 2.7 μm × 2.7 μm) showing a few molecular aggregates on the vertical wall of the S/D electrode (high-pass filtered). f) Ca. 99 nm pentacene in the cBC configuration. g) Topographic profiles along the lines in (a) (black curve) and (d) (red curve). h) Topographic profiles along the lines in (b) (black curve) and (e) (red curve). i) Topographic profiles along the lines in (c) (black curve) and (f) (red curve).
(Fig. 2e) were disrupted by the presence of ca. 33 nm of S/D electrode. The electrode-induced discontinuities in the pentacene film were still clearly observed even for a thick film (about 99 nm in Fig. 2f and i). The discontinuity seriously influenced charge injection and transport at the electrode/channel interface. As a consequence of the preferential orientation and the grain overlapping, the electrical contact at the electrode/channel interface was dramatically improved. This was evident from the linear behavior in the small bias range (Fig. 1c) and smaller threshold voltage ($V_T$; Table 1) of the pBC transistor, in contrast to the nonlinear behavior in the small bias range (Fig. 1f) and large $V_T$ of the cBC transistor.

Compared with the cBC configuration, the present pBC configuration for OTFTs has striking advantages such as high performance and low cost, because a potentially thinner organic active layer (down to 5–10 nm) can be used. For example, the saturation mobilities of our pBC and cBC transistors with about 7 nm of pentacene are 0.32 and 0.09 cm² V⁻¹ s⁻¹, respectively. In view of the physical contact between the S/D electrodes and the organic active layer, the present pBC configuration can be regarded as an inverted ‘TC configuration’ and could be considered equivalent to a TC configuration. However, it is almost impossible to avoid metal diffusion into the underlying organic active layer during deposition of the S/D electrodes in the TC configuration, and metal diffusion deteriorates device performance.

(Fig. 3) The orientation distribution of the pentacene grains adjacent to the S/D electrodes in a) pBC configuration and b) cBC configuration. The measurements (in total 2 x 111 grains) are based on four devices with different pentacene thicknesses. $\theta$ is the angle between the edge of the S/D electrode and the long axis of the pentacene grain, as defined in Figure 2b and e. The bars show the experimental measurements and the dashed curves show the Gaussian fit to them.
In summary, we have demonstrated a novel and universal planarized BC configuration for high-performance OTFT fabrication. The mobility of the pentacene pBC-OTFTs is much higher than that of our control transistors, and comparable with the best values of TC-OTFTs on SiO₂/Si reported to date. The pronounced improvement is mainly attributed to the in-plane orientational growth of pentacene grains from grapho-epitaxy on an etching-induced SiO₂ edge and an overlap of pentacene grains across the edges of the S/D electrodes. Although this study was conducted for the case of pentacene OTFTs on the most popular SiO₂/Si system, the present planarized BC configuration should be applicable for other materials and fabrication methods used for OTFTs, and could be a significant step towards the commercialization of OTFT technology.

**Experimental**

A heavily doped n-Si (100) wafer was used as the substrate and the gate electrode, and thermally oxidized SiO₂ (300 nm) served as the gate dielectric. The substrates with SiO₂ were sequentially cleaned in acetone, propanol, and deionized (DI) water, and blown dry by using N₂. We used conventional photolithography, etching, and lift-off techniques to define and pattern the S/D electrodes. The S/D electrodes of pBC-OTFTs were embedded in the SiO₂ layer by etching patterned SiO₂ using a buffered HF solution, so as to cause the top surface to be aligned with the SiO₂ surface, as seen in Figure 2a. The deposition of the Cr (ca. 2 nm) adhesive layer and the Pt (ca. 31 nm) S/D electrodes onto the SiO₂ dielectric layer was performed by using dc-sputtering, with Ar as a work gas. After stripping the photoresist, we cleaned the partially completed device by using acetone, propanol, and DI water, and blew it dry by using N₂ again, prior to depositing a pentacene active layer on the Pt/Cr electrodes and the SiO₂ (Fig. 2a and d). The pentacene layer was deposited by using the molecular-beam deposition method [8,9] at a base pressure of 5 × 10⁻¹⁰ torr (1 torr = 133.322 Pa). The growth rate was 0.2–0.4 nm min⁻¹ with a gate dielectric. The substrates with SiO₂ were sequentially cleaned in acetone, propanol, and deionized (DI) water, and blown dry by using N₂. We used conventional photolithography, etching, and lift-off techniques to define and pattern the S/D electrodes. The S/D electrodes of pBC-OTFTs were embedded in the SiO₂ layer by etching patterned SiO₂ using a buffered HF solution, so as to cause the top surface to be aligned with the SiO₂ surface, as seen in Figure 2a. The deposition of the Cr (ca. 2 nm) adhesive layer and the Pt (ca. 31 nm) S/D electrodes onto the SiO₂ dielectric layer was performed by using dc-sputtering, with Ar as a work gas. After stripping the photoresist, we cleaned the partially completed device by using acetone, propanol, and DI water, and blew it dry by using N₂ again, prior to depositing a pentacene active layer on the Pt/Cr electrodes and the SiO₂ (Fig. 2a and d). The pentacene layer was deposited by using the molecular-beam deposition method [8,9] at a base pressure of 5 × 10⁻¹⁰ torr (1 torr = 133.322 Pa). The growth rate was 0.2–0.4 nm min⁻¹ with a substrate temperature of 56 °C. The channel width and length of our pentacene OTFTs is 5000 μm and 22.9 μm, respectively. All the processes were the same for the pBC, eBC, and TC configurations, except for the etching of patterned SiO₂ for pBC and the shadow-mask used to pattern the Au S/D electrodes for the control TC-OTFTs.

The capacitance of the dielectric was around 10 nF cm⁻², which was determined by taking measurements on capacitor test structures with a Keithley Model 595 Quasistatic C–V meter. Current–voltage measurements were determined by taking measurements on capacitor test structures with a Keithley Model 595 Quasistatic C–V meter. Current–voltage measurements were collected using a semiconductor parameter analyzer (Agilent Technologies E5272A equipped with E5281A SMU).

Tapping-mode, contact-mode, and friction-force AFM images were measured by using a JEOL JSPM-5200. For tapping-mode AFM measurement, an Olympus AC240TS cantilever was used. For friction-force images along with contact-mode AFM images, a non-conductive silicon nitride tip (Veeco NP-20; Spring constant of about 0.12 N m⁻¹) was used. The fast-scan direction of the tip was perpendicular to the long axis of the cantilever [17], such that frictional force on the tip exerted a torque about the cantilever’s principal axis, which was measured by using the horizontal-difference signal of the quadrant photodetector.

Statistical analyses of the orientation of the pentacene crystals near the S/D electrodes were performed as follows. In both pBC and eBC cases, we measured the angle between the edge of the S/D electrode and the long axis of the diamond-shaped pentacene grain, as defined in Figure 2b and e. In each case, 111 pentacene grains were measured: they consisted of 33 grains from the device with ca. 3 nm pentacene, 39 grains from the device with ca. 4 nm pentacene, 28 grains from the device with ca. 7 nm pentacene, and 11 grains from the device shown in Figure 2c and Figure 2f. For the thick pentacene layer, as in Figure 2c and f, small grains that did not exhibit a clear shape were excluded. In the thinner pentacene layer, we excluded the small grains appearing without an obvious long axis at that growth stage. As the length percentage occupied by such small grains at electrode/pentacene interface is small, the device performance must be mainly dominated by the larger grains, as shown in the orientation statistics.

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